## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 23-43. The claims are as follows:

## **Listing of Claims:**

1. (Original) An access circuit structure for selectively providing an externally accessible terminal with access to each of a plurality of circuit wells fabricated in a semiconductor substrate and isolated from each other, the access circuit structure comprising for each of the circuit wells:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor; and

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration.

2. (Original) The access circuit structure of claim 1 wherein the first select signal and the second select signal comprise a common select signal.

- 3. (Original) The access circuit structure of claim 1 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.
- 4. (Original) The access circuit structure of claim 3 wherein the substrate comprises an n-type substrate, and the wells in which the first and second transistors are fabricated and the circuit wells comprise respective p-type wells.
- 5. (Original) An access circuit for selectively providing an externally accessible terminal with access to each of a plurality of circuit wells fabricated in a semiconductor substrate and isolated from each other, each of the circuit wells having a respective semiconductor circuit fabricated therein, the access circuit comprising for each of the circuit wells:

a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal, the control circuit comprising:

- a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of the first transistor; and
- a control transistor having a gate terminal coupled to receive the first access signal, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

- 6. (Original) The access circuit of claim 5 wherein the semiconductor circuit fabricated in each of the circuit wells comprises a memory circuit.
- 7. (Original) The access circuit of claim 6 wherein each of the memory circuits comprises a respective dynamic random access memory circuit.
- 8. (Original) The access circuit of claim 6 wherein each of the memory circuits comprises an array of memory cells.
- 9. (Original) The access circuit of claim 8 wherein each of the arrays of memory cells comprises an array of dynamic random access memory cells.
- 10. (Original) The access circuit of claim 5 wherein the second control circuit is identical to the first control circuit.
- 11. (Original) The access circuit of claim 5 wherein the first control circuit further comprises a first switching transistor having a gate terminal coupled to receive the access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.
- 12. (Original) The access circuit of claim 11 wherein the first control circuit further comprises a second switching transistor having a gate terminal coupled to receive a

compliment of the access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.

- 13. (Original) The access circuit structure of claim 5 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.
- 14. (Original) The access circuit of claim 13wherein the substrate comprises a p-type substrate, and the wells in which the first and second transistors are fabricated and the circuit wells comprise respective n-type wells.
- 15. (Original) The access circuit of claim 5 wherein the second control circuit comprises:
- a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of the second transistor; and
- a control transistor having a gate terminal coupled to receive the second access signal, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor.
- 16. (Original) The access circuit of claim 5 wherein the first access signal and the second access signal comprise a common access signal.
- 17. (Original) In a memory device having a plurality of memory array cores each including a memory array fabricated in a respective memory core well formed in a semiconductor substrate and isolated from each other, a plurality of access circuits each of which selectively couples an externally accessible terminal to a respective one of the memory core wells, each of the access circuits comprising:
- a first transistor fabricated in a well formed in the semiconductor substrate that is isolated from the memory core wells, the first transistor having a first source-drain region fabricated in the well and being coupled to the externally accessible terminal and to the well, a second source-drain region fabricated in the well, and a gate electrode fabricated between the

first and second source-drain regions of the first transistor and coupled to receive a first select signal for the respective circuit well, the first transistor being fabricated in the well in a manner that causes a first diode to be formed between the source and drain regions of the first transistor;

a second transistor fabricated in a well formed in the semiconductor substrate that is isolated from the circuit wells, the second transistor having a first source-drain region fabricated in the well and being coupled to the second source-drain region of the first transistor, a second source-drain region fabricated in the well and being coupled to the well and to a respective one of the circuit wells, and a gate electrode fabricated between the first and second source-drain regions of the second transistor and coupled to receive a second select signal for the respective circuit well, the second transistor being fabricated in the well in a manner that causes a second diode to be formed between the source and drain regions of the second transistor, the second diode being coupled to the first diode in a back-to-back configuration;

a first control circuit for applying the first select signal to the gate electrode of the first transistor responsive to a first access signal; and

a second control circuit for applying the second select signal to the gate electrode of the second transistor responsive to a second access signal.

- 18. (Original) The access circuit of claim 17 wherein each of the first and second control circuits comprise:
- a shunt transistor having a gate terminal and a pair of source-drain terminals coupled between the externally accessible terminal and the gate electrode of a respective one of the first and second transistors; and
- a control transistor having a gate terminal coupled to receive a respective one of the first and second access signals, the control transistor having a pair of source-drain terminals coupled between the externally accessible terminal and the gate terminal of the shunt transistor.
- 19. (Original) The access circuit of claim 18 wherein each of the control circuits comprise a first switching transistor having a gate terminal coupled to receive the respective access signal, and a pair of source-drain terminals coupled between a supply voltage and the gate terminal of the control transistor.

- 20. (Original) The access circuit of claim 19, further comprising a second switching transistor having a gate terminal coupled to receive a compliment of the respective access signal, and a pair of source-drain terminals coupled between the supply voltage and the gate terminal of the shunt transistor.
- 21. (Original) The access circuit structure of claim 17 wherein the well in which the first transistor is fabricated is different from the well in which the second transistor is fabricated.
- 22. (Original) The access circuit of claim 21 wherein the substrate comprises a p-type substrate, and the wells in which the first and second transistors are fabricated and the memory core wells comprise respective n-type wells.

23-43. (Canceled)